

said ferroelectric layer, and a side of said thin film, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

5. (Twice Amended) A ferroelectric memory, comprising:
an insulation film having a concave portion at a top surface; and
a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein said laminated body includes a lower electrode layer which is brought into contact with a bottom surface of said concave portion, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, wherein said lower electrode layer and said insulation film at respective top surfaces are planarized flush with each other, and a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

REMARKS

The Office Action mailed October 19, 2001 and the reference cited therein have been carefully considered. Claims 1-5 have been amended in a sincere effort to further clarify the subject matter Applicant regards as the invention.

No new matter has been added to the specification or claims, as amended. Support for this Amendment is found generally within the specification, claims, and drawings, as originally filed.

Specifically, support for the amendments to Claims 1, 4, and 5 is found at page 5, line 21 through page 8, line 4 and page 9, lines 12-20 of the specification and is shown in Figures

taken together with the remarks set forth below, it is respectfully submitted that pending Claims 1-5 are now before the Examiner in condition for favorable consideration and allowance.

Applicant would like to take this opportunity to thank the Examiner for conducting a telephonic interview with the undersigned on February 13, 2002. The Examiner indicated that the amendments to Claims 1-5 and the arguments in support of the patentability of these claims, as submitted herein, appear to distinguish the claimed invention from the art of record. However, the Examiner stated that further consideration and/or search would be required. Accordingly, a Request for Continued Examination is being submitted herewith.

Claims 1-5 have been rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,708,284 to Onishi (*Onishi*). Specifically, the Examiner indicates that *Onishi* discloses a ferroelectric memory device that includes an insulation film 7 having a hollow at a top surface (column 8, lines 14-15) and a laminated body 8a, 8b, 9, and 10 obtained by laminating a plurality of layers on the top surface and etching a region of the plurality of layers corresponding to a region other than the hollow (column 8, lines 20-23). The Examiner further states that the laminated body includes a lower electrode layer 8b, a ferroelectric layer 9 formed on the lower electrode, and an upper electrode layer 10 formed on the ferroelectric layer 9.

Regarding Claim 2, the Examiner indicates that *Onishi* discloses a film 8a formed in the bottom of the hollow, which separates the insulation film and the lower electrode (column 8, line 16). The Examiner states that, regarding Claim 3, *Onishi* discloses a lower electrode layer including a first electrode portion formed at a corner of the hollow and a second electrode portion formed on the first electrode portion, as shown in Figure 6.

laminated body of films 8a and 8b as being IrO_2/Ir rather than $\text{TiN}/\text{Ti}/\text{Pt}$ (column 6, lines 35-55). Therefore, the Examiner concludes that the thin film 8a is formed from the same material as the lower electrode.

Regarding Claim 5, the Examiner states that *Onishi* discloses the lower electrode being planarized to receive the ferroelectric layer, as shown in Figure 6, but does not disclose that the lower electrode is planarized flush with the insulation film. However, the Examiner indicates that, since the criticality of this limitation has not been established, this is merely a design choice.

The subject invention is directed to a ferroelectric memory, which includes an insulation film having a concave portion at a top surface and a laminated body, which is laminated on the top surface. The laminated body includes a plurality of layers on the top surface that are etched in a region corresponding to a region other than the concave portion. Specifically, the laminated body includes a lower electrode layer, which is brought into contact with a bottom surface of the concave portion, a ferroelectric layer formed on the lower electric layer, and an upper electrode layer formed on the ferroelectric layer. A portion of the lower electrode layer protrudes outward from an inner peripheral edge forming the concave portion. A side of the protruding portion of the lower electrode layer, a side of the ferroelectric layer, and a side of the upper electrode layer are flush with each other, as now defined by amended Claim 1.

The subject invention is also directed to a ferroelectric memory, in which the laminated body includes a thin film of a same material as that of the lower electrode layer, which is formed on a surface of the lower electrode layer. The ferroelectric layer is formed on the thin film. A side of the thin film, a side of the ferroelectric layer, and a side of the upper electrode layer are flush with each other, as now defined by amended Claim 4.

The subject invention is further directed to a ferroelectric memory, wherein the lower electrode layer and the insulation film at respective top surfaces are planarized flush with each other. A side of the ferroelectric layer and a side of the upper electrode layer are flush with each other, as now defined by amended Claim 5.

In addition, the subject invention is directed to a ferroelectric memory, which includes an insulation film having a hollow at a top surface and a laminated body laminated on the top surface. The memory includes a film, which separates the insulation film from the lower electrode layer, formed in a bottom of the hollow, as now defined by amended Claim 2.

Further, the subject invention is directed to a ferroelectric memory, which includes an insulation film having a hollow at a top surface and a laminated body laminated on the top surface. The lower electrode layer includes a first electrode portion formed in a corner of the hollow and a second electrode portion formed on the first electrode portion, as now defined by amended Claim 3.

Onishi relates to a method for fabricating a non-volatile memory cell, which includes multiple layers of insulation film formed on a semiconductor substrate, impurity diffusion wells, a bottom gate electrode, a pair of bottom electrode layers, a ferroelectric layer, and a top electrode. As shown in Figure 4, a gate insulation film 2 is formed on the entire surface of a P-type silicon substrate 1, and a first contact hole 4 is formed in the desired region of the gate insulation film 2 by using a resist mask 3.

Next, as shown in Figure 5, an N+-silicon layer is formed over the entire surface of the semiconductor substrate 1 and patterned into the desired configuration to form the gate electrode 5a and the bottom gate electrode 5b. Phosphorus is diffused from the bottom gate electrode 5b, which is formed within the contact hole 4, into the semiconductor substrate 1 to

mask, impurity ions are implanted into the semiconductor substrate 1, which is annealed to form impurity diffusion layers 6a, 6b, 6c.

A second interlayer film 7 of non-doped silicate glass is formed over the entire surface of the semiconductor substrate 1, including the gate electrode 5a and the bottom gate electrode 5b. A second contact hole is formed in the second interlayer film 7 on the bottom gate electrode 5b, and a TiN/Ti film 8a and a Pt film 8b, which together comprise the bottom electrode, are deposited over the entire surface of the interlayer film 7. A PZT film 9 serves as a ferroelectric film and is formed on the Pt film 8b.

The lamination of the PZT film 9, Pt film 8b, and TiN/Ti film 8a is etched into the desired configuration. A third interlayer film 7 is formed over the lamination and a third contact hole is formed in the third interlayer film 7 on the PZT film 9. A Pt film is formed on the interlayer film 7 and patterned into the desired configuration as a top electrode 10.

A fourth interlayer film 7 is formed on the top electrode 10 and a fourth contact hole is formed in a fourth interlayer film 7 on the impurity diffusion layer 6b. A bit line 11 made of an aluminum-based material is deposited on the interlayer film 7 including the fourth contact hole to complete the memory cell shown in Figure 1.

The contact holes formed through the insulation layers 2, 7 in Figures 1 and 7 of *Onishi* collectively extend entirely down to the substrate. However, in the subject invention, the concave portion or hollow extends only a portion of the way through the insulation film and does not extend to the substrate. In addition, that portion of *Onishi* referred to by the Examiner (column 8, lines 14-15) indicates that a contact hole is formed in the interlayer film 7 on the bottom gate electrode 5b. Thus, a plurality of layers is not laminated on the top surface of the insulation film in *Onishi*, as now defined by amended Claims 1-5, but rather on

Claims 1, 4, and 5 have been amended to recite that the insulation film includes a concave portion on a top surface of the insulation film to further clarify the distinctions between the claimed invention and the contact hole or through-hole described in *Onishi*, which extends completely through the insulation films 2, 7. Therefore, *Onishi* does not describe "an insulation layer having a concave portion at a top surface", but rather insulation films with contact holes, as described on column 8, lines 14-15, 24-26, and 30-32, which extend entirely through the insulation films 2, 7 down to the substrate 1.

Thus, in the subject invention, the laminated body is formed on the concave portion such that the "lower electrode layer is brought into contact with a bottom surface of the concave portion", as now defined by amended Claims 1, 4, and 5. In contrast, the contact holes in *Onishi* do not possess a bottom surface since they are holes not concave portions or hollows.

In addition, Claims 1, 4, and 5, as now amended, recite that at least a side of the ferroelectric layer and a side of the upper electrode layer are flush with each other. However, in *Onishi*, the sides of the upper electrode layer 10, as shown in Figure 7, are not flush with sides of the ferroelectric layer 9, layer 8a, or layer 8b.

Regarding Claim 2, a film, which separates the insulation film from the lower electrode layer, is formed in a bottom of the hollow. However, *Onishi* does not describe a bottom of a hollow since the contact holes shown in Figures 4-7 of *Onishi* do not have a bottom surface. In addition, if the Examiner equates the bottom of the contact holes with the bottom of the hollow, layer 8a still does not separate the insulation films 2, 7 from the lower electrodes 5b, 8b, since *Onishi* describes a through-hole, wherein the lower electrodes 5b, 8b are completely surrounded by the insulation films 2, 7.

5, *Onishi* does not describe a hollow or concave portion, but rather describes a contact hole that extends entirely through the insulation films 2, 7 down to the substrate 1 or impurity diffusion wells 6a, 6b, 6c within the substrate 1, as described at column 8, lines 11-23.

Applicant respectfully notes that in order to support a claim of *prima facie* anticipation, a single reference must teach or enable each of the claimed elements as arranged in the claim interpreted by one of ordinary skill in the art. Further, in order to support a claim of *prima facie* obviousness, the cited references must teach or suggest each and every element of the invention, and there must be a motivation in the references or the prior art to combine the references as suggested.

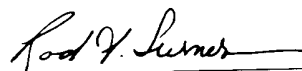
However, none of the art of record teaches or suggests, either alone or in combination, a ferroelectric memory, which includes an insulation film having a concave portion at a top surface and a laminated body laminated on the top surface, wherein the lower electrode layer is brought into contact with a bottom surface of the concave portion and a side of the ferroelectric layer and a side of the upper electrode layer are flush with each other, as now defined by amended Claims 1, 4, and 5. In addition, none of the art of record teaches or suggests a ferroelectric memory, which includes an insulation film having a hollow at a top surface and a laminated body laminated on the top surface, which includes a film formed at a bottom of the hollow that separates the insulation film and the lower electrode layer, as now defined by amended Claim 2.

Further, none of the art of records teaches or suggests a ferroelectric memory, which includes an insulation film having a hollow at a top surface and a laminated body laminated on the top surface, wherein the lower electrode layer includes a first electrode portion formed in a corner of the hollow and a second electrode portion formed on the first electrode portion, as now defined by amended Claim 3. Therefore, it is respectfully requested that the rejection

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In view of the foregoing Amendment and remarks, entry of the amendments to Claims 1-5, favorable consideration of Claims 1-5, as amended, and allowance of pending Claims 1-5 are respectfully and earnestly solicited.

Respectfully submitted,



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VERSION OF AMENDMENT WITH MARKS
TO SHOW CHANGES MADE

1. (Twice Amended) A ferroelectric memory, comprising:
an insulation film having a [hollow] concave portion at a top surface; and
a laminated body obtained by laminating a plurality of layers on said top surface and
etching a region of said plurality of layers corresponding to a region other than said [hollow]
concave portion, wherein said laminated body includes a lower electrode layer which is
brought into contact with a bottom surface of said concave portion, a ferroelectric layer
formed on said lower electrode layer and an upper electrode layer formed on said
ferroelectric layer, wherein a portion of said lower electrode layer protrudes outward from an
inner peripheral edge forming said concave portion, and a side of said portion of said lower
electrode layer, a side of said ferroelectric layer and a side of said upper electrode layer are
flush with each other.

2. (Amended) A ferroelectric memory [according to claim 1], [further]
comprising:
an insulation film having a hollow at a top surface; and
a laminated body obtained by laminating a plurality of layers on said top
surface and etching a region of said plurality of layers corresponding to a region other than
said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric
layer formed on said lower electrode layer and an upper electrode layer formed on said
ferroelectric layer; and the memory further comprising a film formed in a bottom of said
hollow and separating between said insulation film and said lower electrode layer.

3. (Twice Amended) A ferroelectric memory [according to claim 1],
comprising:

a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said hollow, wherein said laminated body includes a lower electrode layer, a ferroelectric layer formed on said lower electrode layer and an upper electrode layer formed on said ferroelectric layer, and [wherein] said lower electrode layer includes a first electrode portion formed at a corner of said hollow and a second electrode portion formed on said first electrode portion.

4. (Twice Amended) A ferroelectric memory [according to claim 1, wherein said lower electrode is formed on a surface thereof with thin film of a same material as that of said lower electrode], comprising:

an insulation film having a concave portion at a top surface; and
a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein said laminated body includes a lower electrode layer which is brought into contact with a bottom surface of said concave portion, thin film of a same material as that of said lower electrode layer formed on a surface of said lower electrode layer, a ferroelectric layer formed on said thin film and an upper electrode layer formed on said ferroelectric layer, and a side of said thin film, a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.

5. (Twice Amended) A ferroelectric memory [according to claim 1, wherein], comprising:

an insulation film having a concave portion at a top surface; and
a laminated body obtained by laminating a plurality of layers on said top surface and etching a region of said plurality of layers corresponding to a region other than said concave portion, wherein said laminated body includes a lower electrode layer which is

formed on said lower electrode layer and an upper electrode layer formed on said

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ferroelectric layer, wherein said lower electrode layer and said insulation film at respective top surfaces are planarized flush with each other, and a side of said ferroelectric layer and a side of said upper electrode layer are flush with each other.